CLAIMS

What we claim is:

1   1.   A device comprising:

2   a central processor and at least one coprocessor coupled to at least one bus;

3   a memory device coupled to the bus; and

4   at least one register coupled to the bus and including information for use in

5 controlling at least one configuration of the memory device in response to system state

6 information, a first configuration supporting direct access to the memory device

7 exclusively by the coprocessor, a second configuration supporting at least one of direct

8 access to a first area of the memory device by the coprocessor and indirect access to a

9 second area of the memory device by the central processor, and a third configuration

10 supporting at least one of direct access to the first area of the memory device by the

11 coprocessor and direct access to a third area of the memory device by the central

12 processor.

1   2.   The device of claim 1, further comprising at least one decoder coupled to the at

2 least one bus, the decoder using address information on the bus to select one of the

3 memory areas to receive data corresponding to the address information.

1   3.   The device of claim 1, further comprising at least one bridge unit that couples the

2 coprocessor and the memory device to a first bus, wherein the indirect access to the

3 memory device by the central processor includes mapping at least one set of memory

4 locations of the memory device through the bridge unit for access by the central

5 processor.

1   4.   The device of claim 1, further comprising at least one memory interface that

2 couples the memory device to a first bus, wherein the direct access to the memory device

3 by the central processor includes mapping at least one set of memory locations of the

4 memory device through the memory interface for access by the central processor.

1   5.   The device of claim 1, wherein the central processor is clocked at a first speed and

2   the coprocessor is clocked at a second speed.

1   6.   The device of claim 1, wherein the at least one bus includes:

2   a first bus coupling the central processor to a bridge unit;

3   a second bus coupling the bridge unit to the coprocessor and the memory device.

1   7.   The device of claim 1, wherein the device includes at least one of cellular

2   telephones, portable position tracking devices, and cellular telephones coupled to position

3   tracking devices.

1   8.   An electronic system comprising:

2   a first memory area coupled for access by a first processor via a first bus;

3   a second memory area coupled for access by a second processor via a second bus;

4   and

5   at least one memory configuration that supports shared access of the second

6   memory area by the first processor, wherein the at least one configuration includes access

7   by the first processor to a first set of memory locations of the second memory area via the

8   first bus and access by the first processor to a second set of memory locations of the

9   second memory area via the second bus.

1   9.   The system of claim 8, wherein the first processor is a central processor running

2   in a first clock domain and the second processor is a digital signal processor (DSP)

3   running in a second clock domain.

1   10.   The system of claim 8, further comprising at least one decoder coupled to receive

2   information on the first bus, wherein the decoder uses at least one address of the

3   information to select access to the first and second memory areas.

1   11.   The system of claim 10, wherein the decoder selects the first memory area for

2   access by data having an address in a first address range.

1   12.   The system of claim 11, wherein the decoder selects the second set of memory

2   locations of the second memory area for access by data having an address in a second

3   address range.

1   13.   The system of claim 11, wherein the decoder selects the first set of memory

2   locations of the second memory area for access by data having an address in a third

3   address range, wherein the third address range is a first subset of addresses of the second

4   address range.

1   14.   The system of claim 11, wherein the decoder selects the first set of memory

2   locations of the second memory area for access by data having an address in a fourth

3   address range, wherein the fourth address range is a second subset of addresses of the

4   second address range.

1   15.   The system of claim 8, further comprising at least one configuration register that

2   stores information including at least one memory configuration.

1   16.   The system of claim 8, wherein the first set of memory locations includes at least

2   one memory block clocked at a speed approximately equal to a clock speed of the first

3   processor.

1   17.   The system of claim 8, wherein the second set of memory locations includes at

2   least one memory block clocked at a speed approximately equal to a clock speed of the

3   second processor.

1   18.   The system of claim 8, further comprising at least one bridge unit that couples the

2   first bus and the second bus, wherein access by the first processor to the second set of

3   memory locations of the second memory area via the second bus includes mapping the

4   second set of memory locations to the first memory area through the bridge unit.

1   19.   The system of claim 8, further comprising at least one memory interface that
2 couples to the first bus and the second memory area, wherein access by the first processor
3 to the first set of memory locations of the second memory area via the first bus includes
4 mapping the first set of memory locations to the first memory area through the memory
5 interface.

1   20.   The system of claim 8, wherein the apparatus is at least one of portable
2 communication devices, portable position tracking devices, cellular telephones, cellular
3 telephones coupled to position tracking devices, cellular telephones including position
4 tracking devices, mobile electronic devices, mobile communication devices, personal
5 digital assistants, and processor-based devices.

1   21.   A portable electronic apparatus comprising:
2   a central processor;
3   a signal processor;
4   a first memory area coupled for access by the central processor via a first bus;
5   a second memory area coupled for access by the signal processor via a second
6 bus; and
7   at least one component coupled to the central processor that controls shared
8 access to the second memory area by the central processor, the shared access including
9 access by the signal processor and at least one of indirect access by the central processor
10 to at least one set of memory locations of the second memory area via the second bus and
11 direct access by the central processor to the set of memory locations of the second
12 memory area via the first bus.

1   22.   A method comprising:
2   receiving state information associated with an electronic system; and
3   configuring a memory device using at least one configuration in response to the
4 state information, a first configuration supporting direct access to the memory device
5 exclusively by a coprocessor, a second configuration supporting at least one of direct
6 access to a first area of the memory device by the coprocessor and indirect access to a

7 second area of the memory device by a central processor, and a third configuration

8 supporting at least one of direct access to the first area of the memory device by the

9 coprocessor and direct access to a third area of the memory device by the central

10 processor.

1 23. The method of claim 22, further comprising:

2 receiving address information associated with data of the electronic system;

3 decoding the address information; and

4 selecting one of the areas of the memory device to receive the data in response to

5 the decoded address information.

1 24. The method of claim 22, further comprising mapping at least one set of memory

2 locations of the memory device through a first interface to provide the indirect access to

3 the memory device by the central processor.

1 25. The method of claim 22, further comprising mapping at least one set of memory

2 locations of the memory device through a second interface to provide the direct access to

3 the memory device by the central processor.

1 26. The method of claim 22, further comprising:

2 clocking the direct access at a first clock speed; and

3 clocking the indirect access at a second clock speed.

1 27. A method for providing shared access to a memory area, comprising:

2 receiving data and corresponding address information;

3 accessing a first memory area when the address information indicates the data is

4 of a first type;

5 accessing a first block of a second memory area when the address information

6 indicates the data is of a second type; and

7   accessing at least one set of memory locations of a second block of the second

8   memory area when the address information indicates the data is the first type and the

9   address exceeds a boundary of at least one address range.

1   28.   A method for controlling memory access in an electronic system, comprising:

2   receiving state information of the electronic system;

3   automatically reallocating at least one address block of a first memory area in

4   response to the state information;

5   receiving data and corresponding address information;

6   accessing a second memory area when the address information indicates the data

7   is of a first type and accessing the first memory area when the address information

8   indicates the data is of a second type; and

9   accessing the at least one address block of the first memory area when the address

10   information indicates the data is the first type and the address exceeds a boundary of at

11   least one address range.

1   29.   A processor-based device, comprising:

2   means for receiving data and corresponding address information;

3   means for accessing a first memory area when the address information indicates

4   the data is of a first type;

5   means for accessing a first block of a second memory area when the address

6   information indicates the data is of a second type; and

7   means for accessing at least one set of memory locations of a second block of the

8   second memory area when the address information indicates the data is the first type and

9   the address exceeds a boundary of at least one address range.

1   30.   A computer readable medium including executable instructions which, when

2   executed in a processing system, cause the system to:

3   receive state information associated with an electronic system; and

4   configure a memory device using at least one configuration in response to the

5   state information, a first configuration supporting direct access to the memory device

6   exclusively by a coprocessor, a second configuration supporting at least one of direct

7   access to a first area of the memory device by the coprocessor and indirect access to a

8   second area of the memory device by a central processor, and a third configuration

9   supporting at least one of direct access to the first area of the memory device by the

10   coprocessor and direct access to a third area of the memory device by the central

11   processor.